IN THE CLAIMS

1. (Allowed) An integrated circuit device on a substrate, comprising:

multiple semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the multiple semiconductor surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, wherein the inner and the pair of outer plugs are formed by the method of:

forming a first opening in a first isolation layer on the multiple semiconductor surface structures, wherein forming the first opening includes exposing portions of the multiple semiconductor surface structures, and includes exposing portions of the substrate between the multiple semiconductor surface structures;

depositing a first conductive material in the first opening to cover the multiple semiconductor surface structures;

forming a second isolation layer across the first conductive material;

etching the first conductive material and the second isolation layer to form a second opening in the first conductive material in a source region on the substrate, wherein the second opening exposes portions of an adjacent pair of the multiple semiconductor surface structures;

forming spacers on interior walls of the second opening, wherein forming the spacers includes separating the first conductive material into the inner plug and the pair of outer plug, wherein the inner plug is isolated beneath and between the adjacent pair, wherein the outer plugs cover part of top portions of the adjacent pair; and

forming a second conductive material in the second opening, whereby the second conductive material contacts the inner plug and is isolated from the outer plugs by the spacers.

2-3. (Canceled)

4. (Allowed) An integrated circuit comprising:

a first surface structure, a second surface structure, a third surface structure, and a fourth surface structure, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug; and

an isolation for covering the inner electrical contact.

5. (Allowed) The integrated circuit of claim 4 further comprising a substrate connected to the first through fourth surface structures, the inner plug, and the first and second outer plugs.

6. (Allowed) The integrated circuit of claim 5, wherein the first through four surface structures are spaced apart along the substrate.

7. (Allowed) The integrated circuit of claim 4 further comprising a first outer contact region connected to the first outer plug.

8. (Allowed) The integrated circuit of claim 7, wherein the first contact region is tapered.

9. (Allowed) The integrated circuit of claim 8 further comprising a second outer contact region connected to the second outer plug.

10. (Allowed) The integrated circuit of claim 4, wherein the first and second outer plugs are on opposing sides of the inner plug.

11. (Allowed) The integrated circuit of claim 10, wherein the first and second spacers are located on opposing sides of the inner plug.

12-31. (Canceled)

32. (Allowed) An integrated circuit comprising:

a plurality of surface structures, each of the surface structures having a top surface;

an inner plug formed between a pair of surface structures among the plurality of surface structures, and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug;

a pair of outer plugs, each outer plug of the pair of outer plugs having an upper portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers formed between the pair of outer plugs and the inner plug and the inner electrical contact.

33. (Allowed) The integrated circuit of claim 32, further comprising an isolation layer formed around the inner electrical contact, the isolation layer being formed from insulating material.

34. (Allowed) The integrated circuit of claim 32, wherein the inner plug is formed from conductive material.

35. (Allowed) The integrated circuit of claim 34, wherein the pair of outer plugs are formed from conductive material.

36. (Allowed) The integrated circuit of claim 32, wherein the pair of spacers are formed from insulating material.

37. (Allowed) The integrated circuit of claim 32, wherein:

a first outer plug of the pair of outer plugs is formed on one side the inner plug; and

a second outer plug of the pair of outer plugs is formed on another side the inner plug.

38. (Allowed) The integrated circuit of claim 32, wherein:

a first spacer of the pair of spacers is formed on one side the inner plug; and

a second spacer of the pair of spacers is formed on another side the inner plug.

39. (Allowed) The integrated circuit of claim 32, wherein the surface structures are formed from semiconductor material.

40. (Allowed) An integrated circuit comprising:

a plurality of surface structures formed over a substrate, each of the surface structures having a top surface;

an inner plug formed between a pair of surface structures among the plurality of surface structures and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug;

a first outer plug and a second outer plug, each of the first and second outer plugs having an upper portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers, each spacer of the pair of pacers having a spacer portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures for isolating the inner plug and the inner electrical contact from the first and second outer plugs.

41. (Allowed) The integrated circuit of claim 40, further comprising an isolation structure formed around the inner electrical contact, the isolation structure being formed from insulating material.

42. (Allowed) The integrated circuit of claim 41, further comprising an isolation layer formed over the first and second outer plugs.

43. (Allowed) The integrated circuit of claim 40, wherein the inner plug is formed from conductive material.

44. (Allowed) The integrated circuit of claim 43, wherein the pair of spacers are formed from insulating material.

45. (Allowed) The integrated circuit of claim 40 further comprising:

a first contact region formed through the isolation layer and connected to the first outer plug; and

a second contact region formed through the isolation layer and connected to the second outer plug.

46. (Allowed) The integrated circuit of claim 45, wherein the first and second outer plugs are formed from conductive material.

47. (Allowed) The integrated circuit of claim 46, wherein the first and second contact regions are formed from conductive material.

48. (Allowed) The integrated circuit of claim 47, wherein each of the first and second contact regions is tapered.

49. (Allowed) An integrated circuit comprising:

a plurality of surface structures formed over a substrate each of the of surface structures having a top surface;

an inner plug of conductive material formed between a pair of surface structures among the plurality of surface structures and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug for proving electrical connection to the inner plug, wherein the inner electrical contact is buried in an isolation layer;

a first outer plug of conductive material and a second outer plug of conductive material, each of the first and second outer plugs having an upper portion covering at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers of insulating material formed between the inner plug and the inner electrical contact and the first and second outer plugs.

50. (Allowed) The integrated circuit of claim 49, wherein the inner electrical contact forms a conductive line for electrically connecting to the storage node plugs via the substrate.

51. (Allowed) The integrated circuit of claim 49, wherein the surface structures includes a plurality of conductive lines for creating electrical contacts between the inner electrical contact and the first and second storage node plugs and via the substrate.

52. (Allowed) The integrated circuit of claim 49 further comprising a second isolation layer formed over the first and second outer plugs.

53. (Allowed) The integrated circuit of claim 52 further comprising:

a first contact region formed through the isolation layer and connected to the first outer plug; and

a second contact region formed through the isolation layer and connected to the second outer plug.

54. (New) An integrated circuit comprising:

a substrate;

a first, a second, a third, and a fourth surface structure located on the substrate, each having a top surface;

an inner plug connected to the substrate, the inner plug being located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a first outer plug connected to the substrate, the first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a second outer plug connected to the substrate, the second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug;

an isolation for covering the inner electrical contact; and

an outer contact region connected to the first outer plug.

55. (New) The integrated circuit of claim 54 further comprising another outer contact region connected to the second outer plug.

56. (New) The integrated circuit of claim 54, wherein the first and second outer plugs are on opposing sides of the inner plug.

57. (New) The integrated circuit of 54, wherein the first and second spacers are located on opposing sides of the inner plug.

58. (New) An integrated circuit comprising:

a substrate;

first and second surface structures located on the substrate, each having a top surface;

a contact plug connected to the substrate, the contact plug being located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of storage node plugs, each being connected to the substrate, each of the storage node plugs having an upper portion covered a portion of the top surface of one of the first and second surface structures;

a conductive line connected to the contact plug; and

a pair of spacers for separating the contact plug and the conductive line from the pair of storage node plugs.

59. (New) The integrated circuit of claim 58 further comprising a first storage node connected to one of the storage node plugs.

60. (New) The integrated circuit of claim 59 further comprising a second storage node connected to the other storage node plug.

61. (New) The integrated circuit of claim 58, wherein storage node plugs are on opposing sides of the contact plug.

62. (New) The integrated circuit of claim 58, wherein the pair of spacers are located on opposing sides of the contact plug.

63. (New) An integrated circuit comprising:

a first circuit; and

a second circuit connected to the first circuit, the second circuit including:

a first, a second, a third, and a fourth surface structure, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug; and

an isolation for covering the inner electrical contact.

64. (New) The integrated circuit of claim 63 further comprising a first outer contact region connected to the first outer plug.

65. (New) The integrated circuit of claim 64, wherein the first contact region is tapered.

66. (New) The integrated circuit of claim 65 further comprising a second outer contact region connected to the second outer plug.

67. (New) The integrated circuit of claim 63, wherein the first and second outer plugs are on opposing sides of the inner plug.

68. (New) The integrated circuit of claim 67, wherein the first and second spacers are located on opposing sides of the inner plug.

69. (New) An integrated circuit comprising:

a first circuit; and

a second circuit connected to the first circuit, the second circuit including:

a substrate;

first and second surface structures located on the substrate, each having a top surface;

a contact plug connected to the substrate, the contact plug being located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of storage node plugs, each being connected to the substrate, each of the storage node plugs having an upper portion covered a portion of the top surface of one of the first and second surface structures;

a conductive line connected to the contact plug; and

a pair of spacers for separating the contact plug and the conductive line from the pair of storage node plugs.

70. (New) The integrated circuit of claim 69 further comprising a first storage node connected to one of the storage node plugs.

71. (New) The integrated circuit of claim 70 further comprising a second storage node connected to the other storage node plug.

72. (New) The integrated circuit of claim 69, wherein storage node plugs are on opposing sides of the contact plug.

73. (New) The integrated circuit of claim 69, wherein the pair of spacers are located on opposing sides of the contact plug.